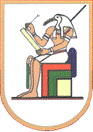
Fall 2010 Faculty of Engineering

Cairo University

Computer Engineering Department

**Logic Design**

CMP 101

Term project (Design report)

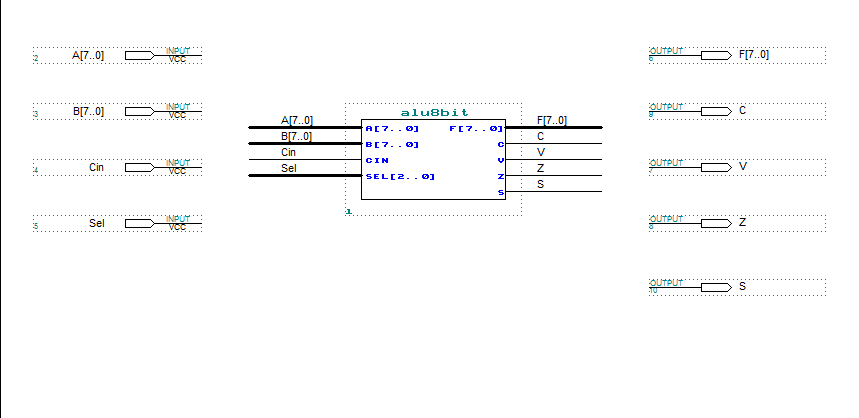
ALU

Group #4

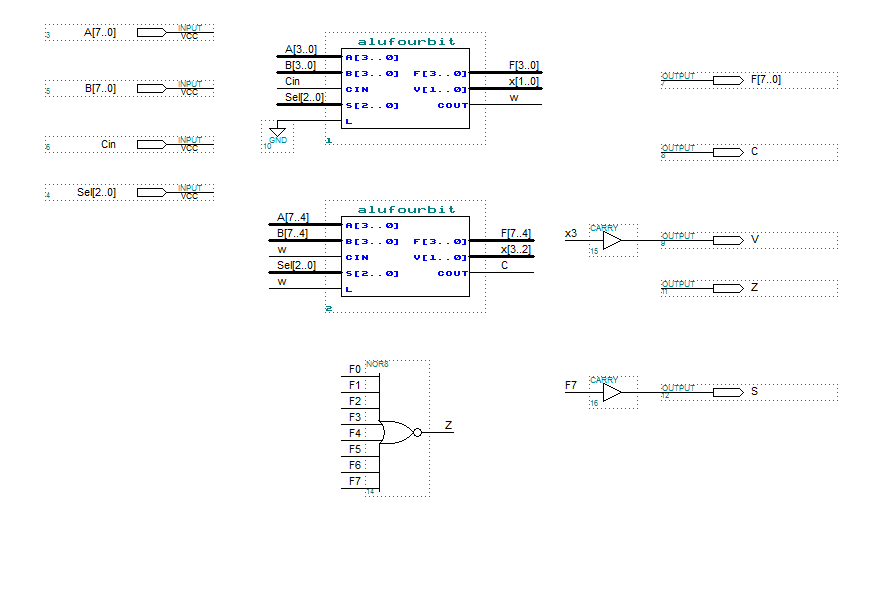
* Ahmed Talaat
* Hasnaa Mohamed
* Esraa Sabry
* Mohamed Sherif

High Level Block Diagram

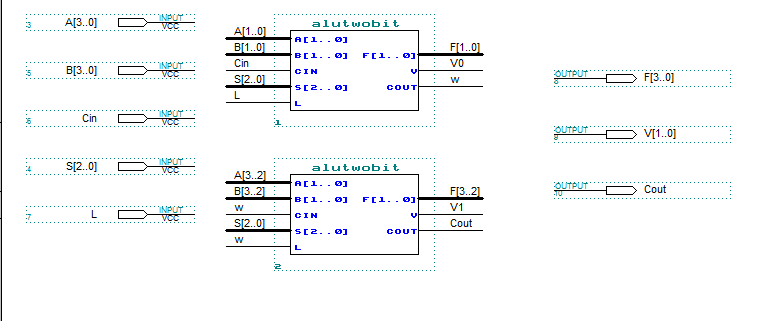
**ALU**



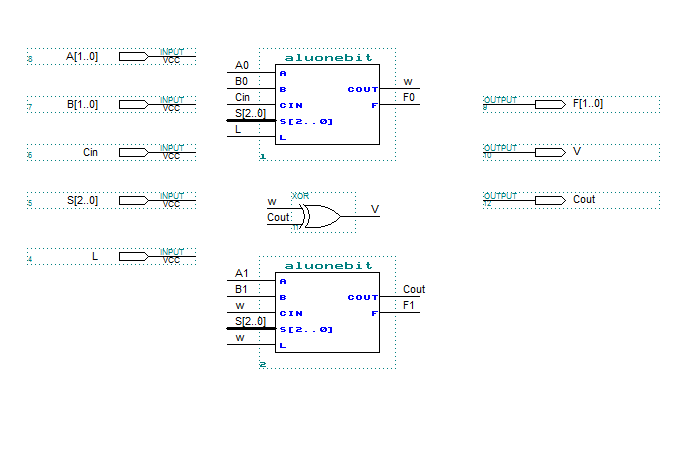
**Alu 8 bit**



**Alu 4 bit**

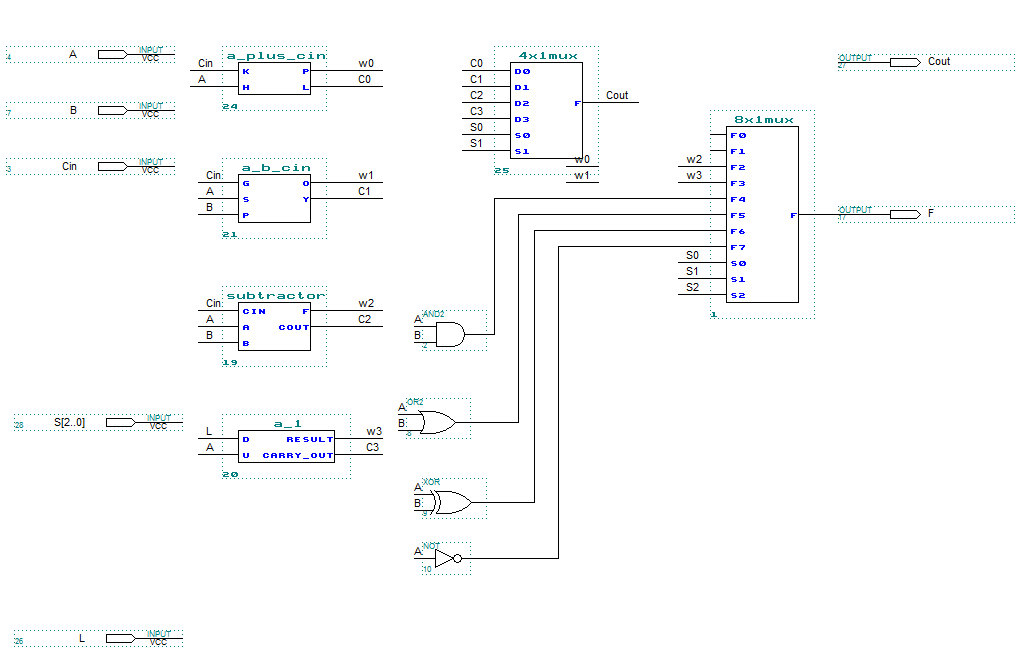
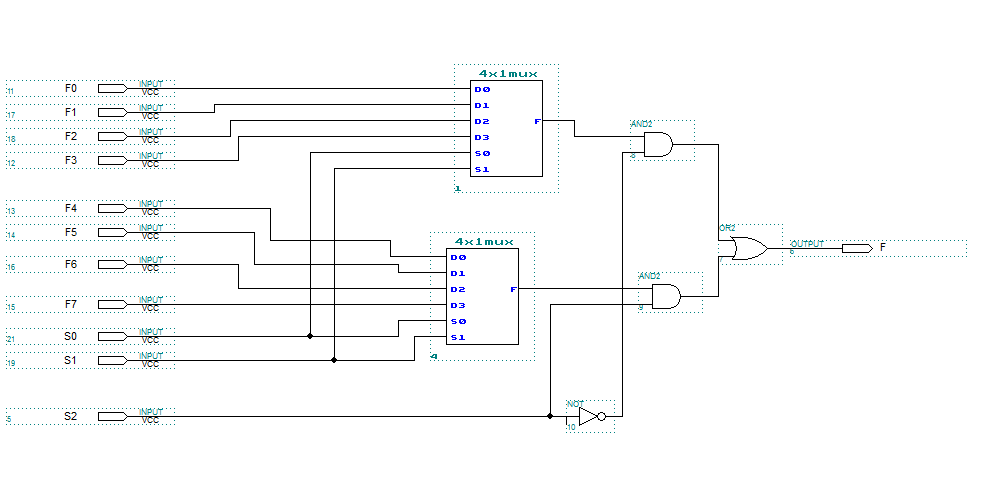


**Alu 2 bit**



**Q**

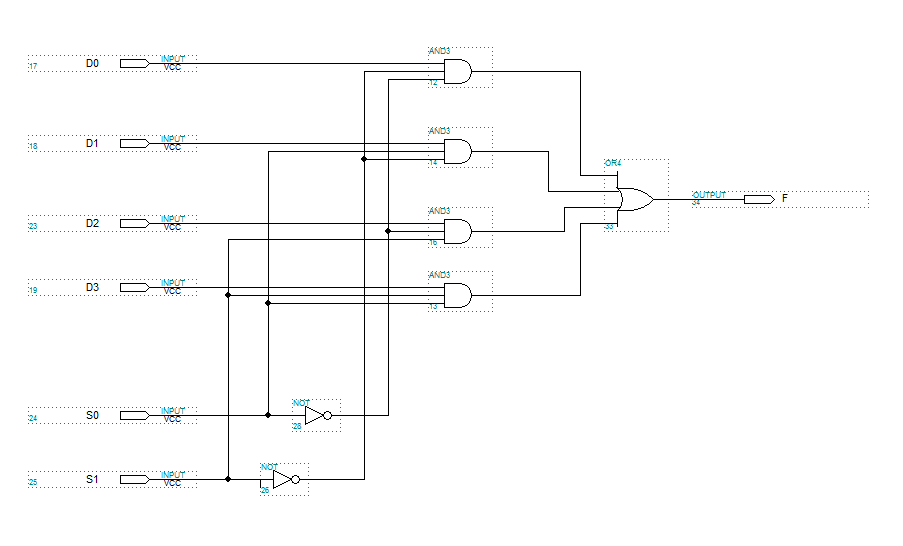
**Alu 1 bit**

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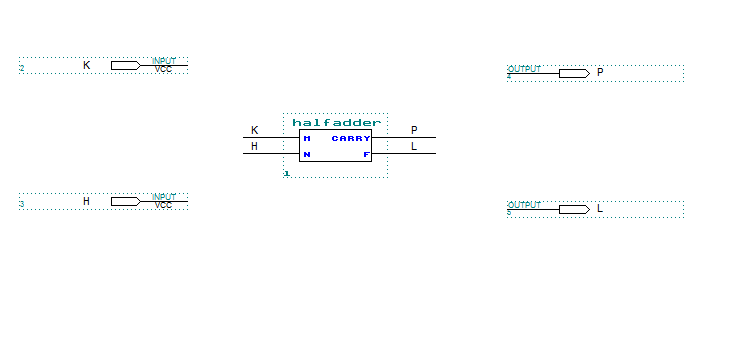
**MUX 8\*1**

Detailed circuit Diagram

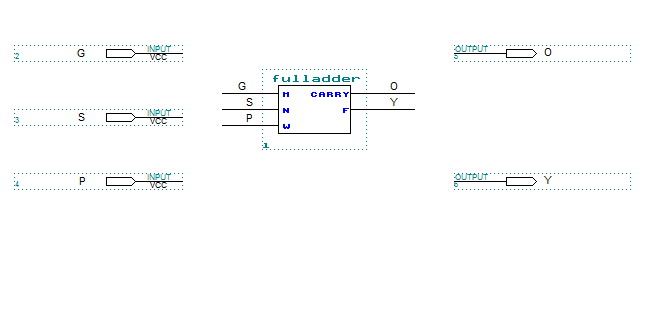
**MUX 4\*1**



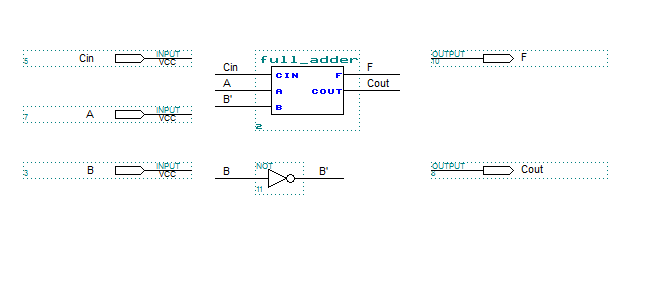
**Increment**



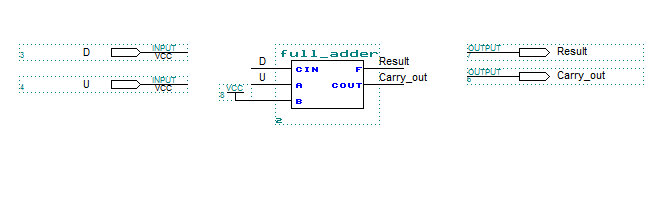
**Addition**

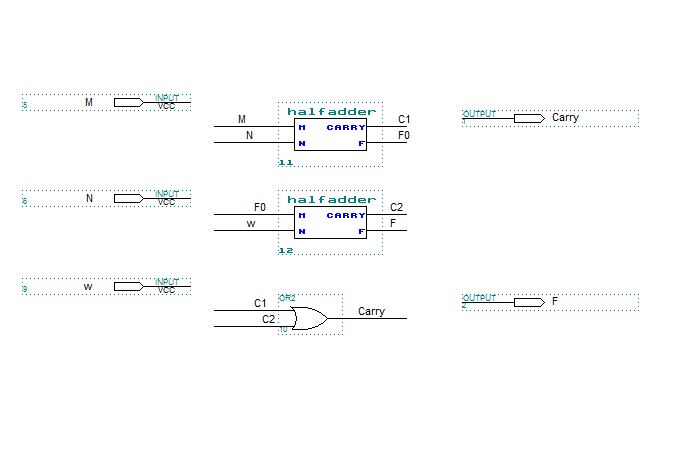
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**Subtraction**



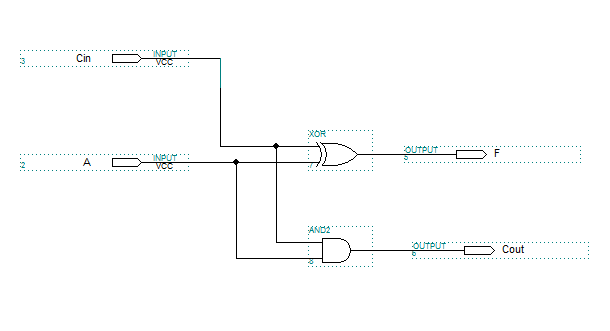
**Decrement**



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**Full Adder**

**Half Adder**



**Details of ALU (number of gates in each block):**

* **8 bit ALU(7 NOR, 68 XOR, 272 AND, 112 OR, 72 NOT):**
  + - **4 bit ALU.**
    - **4 bit ALU.**
    - **7 NOR.**
* **4 bit ALU(34 XOR, 136 AND, 56 OR, 36 NOT):**
  + - **2 bit ALU.**
    - **2 bit ALU.**
* **2 bit ALU(17 XOR, 68 AND, 28 OR, 18 NOT):**
  + - **1bit ALU.**
    - **1bit ALU.**
    - **1 XOR.**
* **1bit ALU(8 XOR, 34 AND, 14 OR, 9 NOT):**
  + - **MUX:**
      * **4\*1 MUX:**
        + 8 AND.
        + 3 OR.
        + 2 NOT.
      * **8\*1 MUX:**
        + 18 AND.
        + 7 OR.
        + 5 NOT.
    - **Increment/transfer (Half Adder):**
      * 1 XOR.
      * 1 AND.
    - **Addition(Full Adder):**
      * 2 XOR.
      * 2 AND.
      * 1 OR.
    - **Subtraction(Full Adder):** 
      * 2 XOR.
      * 2 AND.
      * 1 OR.
      * 1 NOT.
    - **Decrement(Full Adder):**
      * 2 XOR.
      * 2 AND.
      * 1 OR.
    - **1 AND.**
    - **1 OR.**
    - **1 XOR.**
    - **1 NOT.**

**Number of IC’s used in the ALU8Bit:**

* 12 - 7404 HEX Inverters IC’s.
* 28 - 7432 Quad 2-input OR IC’s.
* 68 - 7408 Quad 2-input AND IC’s.
* 17 - 7486 Quad 2-input XOR IC’s.
* 2 – 7402 Quad 2-input NOR IC’s